RÉSUMÉ

Farid N. Najm

Professor
Dept. of Electrical and Computer Engineering
University of Toronto, 10 King's College Rd.
Toronto, Ontario, Canada M5S 3G4
Tel: (416) 946-5175, Fax: (416) 946-8734
Email: f.najm@utoronto.ca
Web: www.ece.utoronto.ca/people/najm-f-n

EDUCATION :

1986-1989: University of Illinois at Urbana-Champaign — Urbana, Illinois, USA

Ph.D. degree, Electrical Engineering. Thesis topic: "Probabilistic Simulation for Reliability Analysis of VLSI Circuits," supervised by Prof. Ibrahim N. Hajj and Dr. Ping Yang, of Texas Instruments Inc. Research conducted in-part at Texas Instruments in Dallas, Texas.

1985–1986: University of Illinois at Urbana-Champaign — Urbana, Illinois, USA

M.S. degree, Electrical Engineering. Thesis topic: "Switch-Level Test Generation for MOS VLSI Circuits," supervised by Prof. Ibrahim N. Hajj.

1979–1983: American University of Beirut — Beirut, Lebanon

B.E. degree (with distinction), Electrical Engineering. Employed as a part-time teaching assistant in the Electrical Engineering Department.

WORK EXPERIENCE :

Since 1999 : University of Toronto — Toronto, Ontario, Canada

Professor (since 2001), served as Department Chair (2009-2019) and Vice-Chair (2004–2007), Associate Professor (1999–2001), with the Edward S. Rogers Sr. Department of Electrical and Computer Engineering (ECE). Research interests include Computer-Aided Design (CAD) techniques for integrated circuits, with the goal of contributing to design methodologies for power estimation and modeling, power supply integrity, timing verification under statistical variability, and reliability in metal lines.

1992–1999 : University of Illinois at Urbana-Champaign — Urbana, Illinois, USA

Assistant Professor 1992–1997, then tenured Associate Professor 1997–1999, with the Electrical and Computer Engineering Department and the Coordinated Science Laboratory. Conducted research on power estimation and modeling for VLSI circuits, synthesis and optimization for low-power, ultra low-power circuits, and integrated circuits reliability.

1987–1992 : Texas Instruments Inc. — Dallas, Texas, USA

Member of Technical Staff with the Semiconductor Process and Design Center (SPDC) at Texas Instruments. Worked with Dr. J.-H. Chern and Dr. Ping Yang, in the general areas of technology CAD, design for manufacturing, design-in reliability, and reliability analysis.

PERSONAL BACKGROUND :

Dual citizen of the US and Canada, originally from Lebanon.

HONOURS/AWARDS :

14. **IEEE/ACM William J. McCalla ICCAD Best Paper Award**, IEEE/ACM International Conference on Computer-Aided Design, November 2020.
13. **Safwat Zaky Research Leader Award**, Faculty of Applied Science & Engineering, University of Toronto, 2020.
12. **IEEE/ACM William J. McCalla ICCAD Best Paper Award**, IEEE/ACM International Conference on Computer-Aided Design, November 2019.
11. **IEEE/ACM William J. McCalla ICCAD Best Paper Award**, IEEE/ACM International Conference on Computer-Aided Design, November 2016.
10. **DAC Prolific Author Award**, for publishing over 30 papers at the Design Automation Conference (DAC), awarded June 5, 2013.
9. **Fellow of the Canadian Academy of Engineering (CAE)**, June 2010.
8. American University of Beirut (AUB), Faculty of Engineering and Architecture (FEA), **The FEA Distinguished Alumnus Award**, *in recognition of groundbreaking contributions to computer-aided design techniques for power management in integrated circuits*, May 2007.
7. Semiconductor Research Corporation (SRC) **Inventor Recognition Award**, 2005, for a patent submission on a low-leakage FPGA routing switch, with Navid Azizi.
6. **Fellow of the IEEE**, *for contributions to estimation and modeling of power dissipation in integrated circuits*, January 2003.
5. Semiconductor Research Corporation (SRC) **Inventor Recognition Award**, 2003, for a patent submission on a low-leakage asymmetric-cell SRAM, with Navid Azizi and Andreas Moshovos.
4. University of Illinois ECE Faculty **Outstanding Teaching Award**, 1999. Also, named, in 1997, to the "Incomplete list of teachers ranked excellent by their students."
3. National Science Foundation (NSF) **Faculty Early Career Development Award** (CAREER). Award of US$200,000, in 1996, to fund work on reliability engineering for integrated circuits.
2. National Science Foundation (NSF) **Research Initiation Award** (RIA). Award of US$100,000, in 1993, to fund work on synthesis of reliable and low power VLSI circuits.
1. IEEE Transactions on CAD **Best Paper Award**, in 1992, for the paper "Probabilistic Simulation for Reliability Analysis of CMOS VLSI Circuits," published in the April 1990 issue.

PATENTS :

Issued:

2. F. N. Najm, A. Moshovos, and N. Azizi, "Low Leakage Asymmetric SRAM Cell Devices," *US Patent No. 7,307,905*, supported by the Semiconductor Research Corporation (SRC), December 11, 2007.
1. J. H. Anderson and F. N. Najm, "Leakage Power Optimization for Integrated Circuits," *US Patent No. 6,993,737 B1*, supported by Xilinx Corp., January 31, 2006.

Other Disclosures:

3. F. N. Najm and S. Onaissi, "A Linear-Time Approach for Static Timing Analysis Covering All Process Corners," *Invention Disclosure*, University of Toronto, April 2006.
2. N. Azizi, K. Pagiamtzis, and F. N. Najm, "A Soft-Error Tolerant Content-Addressable Memory (CAM) Using An Error-Correcting Match Scheme," *Invention Disclosure*, University of Toronto, October 2005.
1. F. N. Najm, "A Logic Design Technique for Ultra Low-Power Logic Circuits based on Dynamic Control of the Standby Leakage Current," *Invention Disclosure*, University of Illinois at Urbana-Champaign, June 1996.

INVITED TALKS :

19. F. N. Najm, "Efficient Simulation of Electromigration Damage in Large Chip Power Grids," *16th International Conference on Reliability and Stress-related Phenomena in Nano and Microelectronics*, San Jose, CA, November 4–6, 2019.

18. F. N. Najm, "Managing Design Challenges for Power-Constrained SOCs," *Cadence Speaker Series, Cadence Design Systems*, San Jose, CA, August 19, 2015.

17. F. N. Najm, "Verification and Design of the Power Delivery Network in VLSI Circuits," *CMOS Emerging Technologies Research Symposium*, Vancouver, BC, May 20-22, 2015.

16. F. N. Najm, "Physical Design Challenges in the Chip Power Distribution Network," *International Symposium on Physical Design*, Monterey, CA, March 29-April 1, 2015.

15. F. N. Najm, "Full Chip Statistical Electromigration Checking," *13th International Workshop on Stress-Induced Phenomena in Microelectronics*, Austin, TX, October 15-17, 2014.

14. F. N. Najm, "Verification of the Power Delivery Network in VLSI Circuits," *IEEE International Workshop on High-Performance Chip, Package and Systems*, (Keynote Address), Ottawa, Canada, November 16, 2013.

13. F. N. Najm, "Overview of Vectorless/Early Power Grid Verification," *ACM/IEEE International Conference on Computer-Aided Design*, San Jose, CA, pp. 670-677, November 5-8, 2012.

12. F. N. Najm, "Power Management for VLSI: The History and the Outlook," plenary talk, *IEEE 20th International Conference on Microelectronics*, Sharjah, UAE, Dec. 14–17, 2008.

11. F. N. Najm, "Power Management for VLSI Circuits and the Need for High-Level Power Modeling and Design Exploration," plenary talk, *IEEE/FMCAD Formal Methods in Computer Aided Design*, Austin, TX, Nov. 11-14, 2007.

10. F. N. Najm, "Power Management for VLSI Circuits," *6th Faculty of Engineering and Architecture (FEA) Student Conference*, American University of Beirut, May 23–24, 2007.

9. F. N. Najm, "On the Need for Statistical Timing Analysis," panel discussion, *ACM/IEEE Design Automation Conference*, Anaheim, CA, June 13–17, 2005.

8. F. N. Najm, "Power Estimation and Modeling for VLSI Circuits," *Distinguished Lecture Colloquium*, Dept. of Electrical and Computer Engineering, University of Toronto, Feb. 2, 1999.

7. F. N. Najm, "High-Level Power Estimation and Modeling," Dept. of Electrical Engineering and Computer Science, University of California, Berkeley, April 23, 1998.

6. F. N. Najm, "High-Level Power Estimation and Modeling," *Dept. of Electrical Engineering/Systems*, University of Southern California, March 1998.

5. F. N. Najm, "Low-Power Design Methodology: Power Estimation and Optimization," *Great Lakes Symposium on VLSI*, March 1997.

4. F. N. Najm, "Power Estimation Techniques for Integrated Circuits," *IEEE International Conference on Computer-Aided Design*, San Jose, CA, November 5–9, 1995.

3. F. N. Najm, "Power Estimation Techniques for VLSI Circuits," *ECE Dept. Distinguished Lecture Series*, Carnegie Mellon University, October 1995.

2. F. N. Najm, "Feedback, correlation, and delay concerns in the power estimation of VLSI circuits," *Design Automation Conference*, San Francisco, CA, June 12–16, 1995.

1. F. N. Najm, "A Survey of Power Estimation Techniques in VLSI Circuits," *ECE Dept. Graduate Seminar*, University of Iowa, Feb. 1995.

SERVICE IN PROFESSIONAL SOCIETIES :

13. **Advisory Board Member**, International Conference on Reliability and Stress-Related Phenomena in Nano and Microelectronics (IRSP), 2019.
12. **Executive Committee Member**, International Symposium on Low-Power Electronics and Design (ISLPED), 1999-2013.
11. **Associate Editor**, IEEE Transactions on Computer-Aided Design, 2001–2009.
10. **Associate Editor**, IEEE Transactions on VLSI, 1997–2002.
9. **General Chairman**, International Symposium on Low-Power Electronics and Design, 1999.
8. **Technical Program Co-Chairman**, International Symposium on Low-Power Electronics and Design, 1998.
7. **Technical Committee Member** of:
   - Design Automation Conference (DAC 1998-99, 2006–08)
   - International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (the TAU Workshop) (TAU 2007–08)
   - International Conference on Computer-Aided Design (ICCAD 1995–97, 2001–2003)
   - International Symposium on Low-Power Electronics and Design (ISLPED 1995–2000)
   - International Symposium on Quality Electronic Design (ISQED 2000–2004)
   - Custom Integrated Circuits Conference (CICC 1994)
   - International Conference on Computer Design (ICCD 1999)
   - International Symposium on VLSI Technology, Systems, & Applications, Taiwan (VLSITSA 93)
   - International Workshop on Low Power Design (IWLPD 1994)
6. **Technical Program Chairman**, Great Lakes Symposium on VLSI, University of Illinois, 1997.
5. **Editor**, Simulation and Modeling Column, IEEE Circuits and Devices Magazine, 1995–1997.
4. **Guest Editor**, VLSI Design Journal, 1995.
3. **Guest Editor**, International Journal on High Speed Electronics and Systems, 1995.
2. **Workshop Co-chairman**, Illinois Computer Affiliates Program (ICAP) workshop, University of Illinois at Urbana-Champaign, 1993.
1. **Session Chairman**, on numerous occasions for ICCAD, VLSITSA, DAC, IWLPD, and ISLPED.

SERVICE IN THE UNIVERSITY :

At the University of Toronto

11. Chair, ECE Department, 2009-2019, including chairing the ECE Executive Committee, Advisory Committee, PTR Committee, and membership of the ECE Promotions Committee, the Faculty Chairs and Directors Committee, Executive Committee of Faculty Council, and the University Principals, Deans, Academic Directors and Chairs (PDAD&C) Committee.
10. Member, Examination Committee, Faculty of Applied Science and Engineering, 2008–2009.
9. Vice-Chair, ECE Dept., 2004–2007, including chairing the ECE Promotions Committee, member, Faculty Vice-Dean Search Committee, member, ECE PTR Committee, chair, ECE Computer Systems User Advisory Committee, chair, ECE Awards Committee, member, ECE Advisory Committee and member, ECE Executive Committee
8. Member, Faculty Senior Promotions Committee, 2003–2007
7. Chair, ECE Department Governance Committee, 2003–2004
6. Served on the Strategic Planning Organizing Committee, 2003–2004
5. Chairman of the Computer and Communications Faculty Search Committee, 2002–2003

4. Chairman of the Computer Faculty Search Committee, 2001–2002
3. Chairman of the Computer Engineering Group, 2000–2003
2. Served on the Group Review Committee, 1999–2000
1. Served on the Computer Engineering Group Search Committee, 1999–2000

At the University of Illinois

6. ECE Department Computer Resources and Education Committee, 1999
5. Circuits and Signal Processing Area Committee Chair, 1997–1998
4. ECE Department Curriculum Committee, 1996–1999
3. Served on the ECE Department ABET Accreditation Committee, 1994–1995
2. Served on the ECE Department Graduate Committee, 1994–1995
1. Chairman, CSL Black/Whiteboard Committee, 1992–1993

CONSULTING ACTIVITIES :

20. Mentor Graphics Corp., Fremont, CA, 2013.
19. Member, External Advisory Board for the Department of Electrical and Computer Engineering at the American University of Beirut, Dec. 2008 – Dec. 2010.
18. Nascentric Inc., Austin, TX, 2008.
17. Nascentric Inc., Austin, TX, 2007.
16. Intel Corp., (Visiting Faculty/Consultant) Hillsboro, OR, 2007.
15. Synopsys Inc., Mountain View, CA, 2006.
14. Nascentric Inc., Austin, TX, 2005.
13. Nascentric Inc., Austin, TX, 2004.
12. Intel Corp., (Visiting Faculty/Consultant) Hillsboro, OR, 2003.
11. Silicon Metrics Corporation, Austin, TX, 1999–2003.
10. ATI Technologies Inc., Unionville, ON, 2000.
9. Actel Corp., Sunnyvale, CA, 2000.
8. Taveren Technology, Austin, TX, 1998.
7. Synopsys Corporation, Mountain View, CA, 1997.
6. International Business Machines (IBM) Corporation, Fishkill, NY, 1996, 1997.
5. Synopsys Corporation, Mountain View, CA, 1996.
4. Intel Corp., (Visiting Faculty/Consultant) Folsom, CA, 1996.
3. Texas Instruments Incorporated, Dallas, TX, 1995.
2. Intel Corp., (Visiting Faculty/Consultant) Santa Clara, CA, 1994.
1. Dimensions in Quick Design Turnaround (DQDT), Carlsbad, CA, 1994.

TUTORIALS AND TECHNOLOGY TRANSFER :

5. Full-day tutorial, with B. Krauter (IBM), R. Panda (Freescale), and E. Chiprout (Intel), on "Design and Analysis of High-Performance Package and Die Power Delivery Networks," *ACM/IEEE 44th Design Automation Conference (DAC-07)*, San Diego, CA, June 9, 2007.

4. Full-day tutorial, with A. Devgan (IBM), S. Narendra (Intel), and D. Blaauw (Michigan), on "Leakage Issues in IC Design," IEEE International Conference on Computer-Aided Design, San Jose, CA, November 9–13, 2003.

3. Full-day tutorial, with A. Chandrakasan (MIT) and R. Panda (Freescale), on "Low Voltage/Low Power Design Methodologies and CAD," IEEE International Conference on Computer-Aided Design, November 1999.

2. Technology Transfer Course, "Power Estimation Tools for VLSI Circuits," for the Semiconductor Research Corporation (SRC), University of Illinois, Urbana, IL, June 1996.

1. Short course, "Dynamics of Physical Systems Under Noise," for Texas Instruments Inc., Dallas, TX, March 1994.

UNIVERSITY COURSES TAUGHT :

At the University of Toronto

6. ECE-1777, Computer Methods for Circuit Simulation. A graduate course covering the theoretical and numerical techniques underlying standard circuit simulation, using my textbook on the subject.

5. ECE-451, VLSI Systems. This is a 4th year course. In my first offering of the course, I completely redid the lecture part, using my previous VLSI course at Illinois as a basis. In the 2nd offering, I upgraded the labs so that the students are now using custom IC design software, such as Mentor, Cadence, and Synopsys tools, instead of FPGAs.

4. ECE-1768, Reliability of Integrated Circuits. This is a new graduate course that I developed, along the lines of my reliability course at Illinois.

At the University of Illinois

3. ECE-325, Introduction to VLSI Systems Design. This is a 4th year course, but was also taken by some graduate students. In my first semester on campus, I did a major overhaul of this course, by updating the material and bringing in the latest material from my industrial practice.

2. ECE-342, Microelectronics. This is a 3rd year course taken by about 100 students. I was course director for this course; I was also responsible for selection of a new text and for restructuring the course material.

1. ECE-484, Reliability Engineering for Integrated Circuits. This is a graduate course which I created. My course notes have been incorporated into a textbook on this material, in collaboration with a colleague from Texas Instruments, published by John Wiley and Sons.

GRADUATE STUDENT SUPERVISION :

	Current	Graduated
Ph.D.	0	19
MASc.	2	33

CURRENTLY SUPERVISED :

2. Bijan Shahriari, since September 2020. Working on **MASc**.

1. Carl Chaanin, since September 2019. Working on **MASc**.

PREVIOUSLY SUPERVISED :

At the University of Toronto

40. Adam Issa, 2017–2019, **MASc August 2019** on "A Stochastic Approach to Electromigration Checking for Chip Power Grids."

39. Zahi Moudallal, 2012–2019, **MASc August 2014** on "Generating Current Constraints for Power Grid Safety." **PhD June 2019** on "Voltage-drop and Electromigration in Chip Power Grids." Now at Tensortorrent, Inc. in Toronto.

38. Abdul-Amir Yassine, 2014–2016, **MASc July 2016** on "A Fast Metal Layer Elimination Approach for Power Grid Reduction in Integrated Circuits." Now working on a PhD at the University of Toronto.

37. Mohammad Fawaz, 2011–2017, **MASc August 2013** on "Electromigration Reliability Analysis of Power Delivery Networks in Integrated Circuits." **PhD September 2017** on "Power Grid Verification." Now at Intel, Toronto.

36. Sandeep Chatterjee, 2011–2017, **MASc August 2013** on "Redundancy-Aware Electromigration Checking for Mesh Power Grids." **PhD September 2017** on "Fast and Scalable Physics-Based Electromigration Checking for Power Grids in Integrated Circuits." Worked for two years after graduation with Intel in Toronto; currently with Google in California.

35. Abhishek, 2010–2012, **MASc August 2012** on "Incremental Power Grid Verification." Now at Synopsys in California.

34. Sari Onaissi, 2005-2011, **MASc June 2007** on "A Linear-Time Approach for Static Timing Analysis Covering All Process Corners." **PhD June 2011** on "Circuit Performance Verification and Optimization in the Presence of Variability." Now with Google in California.

33. Nahi Abdul Ghani, 2005-2011, **MASc June 2007** on "Handling Inductance in Early Power Grid Verification." **PhD June 2011** on "Early Verification of the Power Delivery Network in Integrated Circuits." Worked for three years after graduation at Altera, Toronto; currently with Google in California.

32. Pamela Al Haddad, 2009–2011, **MASc April 2011** on "Power Grid Correction using Sensitivity Analysis under an RC Model."

31. Mehmet Avci, 2008–2010, **MASc August 2010** on "Early Dual Grid Voltage Integrity Verification." Now at Altera in Toronto.

30. Meric Aydonat, 2008–2010, **MASc July 2010** on "Power Grid Correction Using Sensitivity Analysis." Worked with Broadcom then IBM in California; currently with GE Healthcare.

29. Ankit Goyal, 2008–2010, **MASc June 2010** on "On-chip Power Grid Verification with Reduced Order Modeling." Now at AMD in Toronto.

28. Khaled R. Heloue, 2003–2010, **MASc June 2005** on "Statistical Timing Analysis under Process Variations," **PhD August 2010** on "Circuit Timing and Leakage Analysis in the Presence of Variability." Now at AMD in Toronto.

27. Imad Ferzli, 2001–2009, **MASc Dec. 2003** on "Power Grid Statistical Analysis and Verification in Presence of Leakage Current Variations," **PhD Feb. 2009** on "Verification and Planning of the Power Delivery Network in Integrated Circuits Under Design Uncertainties." Now at CPPIB in Toronto.

26. Navid Azizi, 2001–2007, **MASc Dec. 2002** on "Low-Leakage Asymmetric-Cell SRAM", **PhD May 2007** on "Challenges in Nanometre Digital Integrated Circuit Design." Now at Altera Corp. in Toronto.

25. Bin Wu, 2001-2006, **PhD June 2006** on "Dynamic Range Estimation and Bitwidth Determination." Now at Freescale Corp. in Phoenix, Arizona.

24. Denis Kouroussis, 2000-2006, **PhD January 2006** on "Power Grid Verification." Now at ATI Technologies, Unionville, Ontario, Canada.

23. Kay Chan, 2003–2005, **MASc August 2005** on "Exploring Spatial Locality in VLSI On-Chip Power Grid." Now at Intellon Corp. in Toronto.

22. Georges Nabaa, 2003–2005, **MASc July 2005** on "Minimization of Threshold-Voltage Variations and Their Impact in Circuits and FPGAs." Now at Actel Corp. in San Jose, California.

21. David Ng, 2003–2005, **MASc July 2005** on "Modeling Circuit-Level Leakage Current Using Algebraic Decision Diagrams." Went on to study law at the University of Toronto.

20. Jason Anderson, 2001–2005, **PhD June 2005** on "Power Optimization and Prediction Techniques for FPGAs." Now at Xilinx Corp. in Toronto.

19. Maha Nizam, 2003–2005, **MASc June 2005** on "Power Grid Voltage Integrity Verification." Graduated and left the country.

18. Rubil Ahmadi, 2001–2003, **MASc 2003** on "Timing Analysis in Presence of Power Supply and Ground Voltage Variations." Now at ATI Technologies in Unionville, Ontario, Canada.

17. Roman Kordasiewicz, 2000–2002, **MASc 2002** on "Timing Verification of PD-SOI Circuits". Went on to do a PhD at McMaster University in Hamilton, Ontario.

16. Mehrdad Shahriari, 2000–2001, **MASc 2001** on "A Gate-Level Timing Model for SOI Circuits". Now at Genum Corp. in Oakville, Ontario, Canada.

At the University of Illinois

15. Kavel Buyuksahin, 1998–2003, **MS 1999** on "High-Level Interconnect Capacitance Estimation", **PhD 2003** on "Early Power Estimation for VLSI Circuits". At Intel Corp., in Portland, OR, USA.

14. Srinivas Bodapati, 1998–2003, **MS 1999** on "Pre-Layout Estimation of Individual Wire Lengths", **PhD 2003** on "Bottom-up High-Level Current Macro-models for Logic Blocks". At Intel Corp., in Santa Clara, CA, USA.

13. Joseph Kozhaya, 1996–2001, **MS 1997** on "Power Estimation for Sequential Circuits", **PhD 2001** on "Analysis and Design of Power and Ground Networks for VLSI Circuits". At IBM Corp., in Burlington, Vermont, USA.

12. Subodh Gupta, 1995–2000, **MS 1997** on "Power Macromodeling for High Level Power Estimation", **PhD 2000** on "Bottom-up High-Level Power Modeling and Estimation". At Cadence Design Systems, Inc., in California, USA.

11. Rouwaida Kanj, 1998–2000, **MS 2000** on "High Level Design Exploration and Optimization". Went on to do a PhD with another Professor at Illinois, then took a position with IBM Austin Research Labs, in Austin, TX.

10. Xiaochun Tan (co-advised with E. Rosenbaum), 1998–2000, **MS 2000** on "Silicon-on-Insulator MOSFET Body Voltage Model for Application in a Timing Simulator". At Freescale Corp. in Illinois.

9. Gilbert Yoh, 1997–1999, **MS 1999** on "A Statistical Model for Electromigration Failures". At Agilent Technologies Inc., in Colorado, USA.

8. Mahadevamurthy Nemani, 1995–1998, **PhD 1998** on "High-Level Power Estimation". At Intel Corp. in California, USA.

7. Luis Amaya (co-advised with P. Krein), 1995–1998, **PhD 1998** on "Simulation and Design of DC to DC Power Converters".

6. Rajendran Panda, 1993–1996, **PhD 1996** on "Synthesis Techniques for VLSI Low-Power Circuits". At Freescale Corp. in Austin, Texas, USA.

5. Jonathan Halter, 1995–1997, **MS 1997** on "A Gate-Level Leakage Power Reduction Method". At Freescale Corp. in Austin, Texas, USA.

4. Vikram Saxena (co-advised with I. Hajj), 1995–1996, **MS 1996** on "Power Estimation for Sequential Circuits". At Synopsys, Inc., in California, USA.

3. Michael Xakellis, 1993–1994, **MS 1994** on "Estimating Node Transition Densities with Statistical Simulation Techniques". At Mercury Interactive Corp. in California, USA.

2. Yimin Zhang, 1993–1994, **MS 1994** on "Estimation of Node Maximum Transition Density". At Intel Corp. in California, USA.

1. Harish Kriplani (co-advised with I. Hajj), 1991–1993, **PhD 1993** on "Worst Case Voltage Drops in Power and Ground Buses of CMOS VLSI Circuits". At Cadence Design Systems, Inc., in California, USA.

PUBLICATIONS :

Books & Book Chapters

[1] G. K. Yeap and F. N. Najm, Editors, *Low Power VLSI Design and Technology*. Singapore: World Scientific Publishing Co., 1996 (ISBN: 9-810-22518-0).

[2] E. A. Amerasekera and F. N. Najm, *Failure Mechanisms in Semiconductor Devices*, 2nd Ed.. Chichester: John Wiley & Sons, 1997 (ISBN: 0-471-95482-9).

[3] F. N. Najm, "Power Estimation and Optimization," in *Encyclopedia of Electrical and Electronics Engineering*. New York, NY: John Wiley & Sons, February 1999.

[4] F. N. Najm, *Circuit Simulation*. Hoboken, NJ: John Wiley & Sons, 2010 (ISBN: 978-0-470-53871-5).

Journal Papers

[1] R. Burch, J. Hall, F. Najm, D. Hocevar, P. Yang, and M. McGraw, "A CAD system for modeling voltage drop and electromigration in VLSI metallization patterns," *Texas Instruments Technical Journal*, vol. 5, no. 3, pp. 74–84, May-June 1988.

[2] F. Najm, R. Burch, P. Yang, and I. Hajj, "Probabilistic simulation for reliability analysis of CMOS VLSI circuits," *IEEE Transactions on Computer-Aided Design*, vol. 9, no. 4, pp. 439–450, April 1990 (Errata in July 1990). **(Best Paper Award)**

[3] F. Najm and I. Hajj, "The complexity of fault detection in MOS VLSI circuits," *IEEE Transactions on Computer-Aided Design*, vol. 9, no. 8, pp. 995–1001, September 1990.

[4] F. Najm, I. Hajj, and P. Yang, "An extension of probabilistic simulation for reliability analysis of CMOS VLSI circuits," *IEEE Transactions on Computer-Aided Design*, vol. 10, no. 11, pp. 1372–1381, November 1991.

[5] F. Najm, "Transition density: a new measure of activity in digital circuits," *IEEE Transactions on Computer-Aided Design*, vol. 12, no. 2, pp. 310–323, February 1993.

[6] R. Burch, F. Najm, P. Yang, and T. Trick, "A Monte Carlo approach for power estimation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 1, no. 1, pp. 63–71, March 1993.

[7] F. Najm, "Low-pass filter for computing the transition density in digital circuits," *IEEE Transactions on Computer-Aided Design*, vol. 13, no. 9, pp. 1123–1131, September 1994.

[8] F. Najm, "A survey of power estimation techniques in VLSI circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 2, no. 4, pp. 446–455, Dec. 1994. **(Invited Paper)**.

[9] H. Kriplani, F. N. Najm, and I. Hajj, "Pattern independent maximum current estimation in power and ground buses of CMOS VLSI circuits: algorithms, signal correlations, and their resolution," *IEEE Transactions on Computer-Aided Design*, vol. 14, no. 8, pp. 998–1012, August 1995.

[10] M. Nemani and F. N. Najm, "Towards a high-level power estimation capability," *IEEE Transactions on Computer-Aided Design*, vol. 15, no. 6, pp. 588–598, June 1996.

[11] F. N. Najm and M. G. Xakellis, "Statistical estimation of the switching activity in VLSI circuits," *VLSI Design*, vol. 7, no. 3, pp. 243–254, 1998.

[12] R. Panda and F. N. Najm, "Post-mapping transformations for low-power synthesis," *VLSI Design*, vol. 7, no. 3, pp. 289–301, 1998.

[13] M. Nemani and F. N. Najm, "High-level area and power estimation for VLSI circuits," *IEEE Transactions on Computer-Aided Design*, vol. 18, no. 6, pp. 697–713, June 1999.

[14] S. Gupta and F. N. Najm, "Power modeling for high level power estimation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 8, no. 1, pp. 18–29, February 2000.

[15] S. Gupta and F. N. Najm, "Analytical models for RTL power estimation of combinational and sequential circuits," *IEEE Transactions on Computer-Aided Design*, vol. 19, no. 7, pp. 808–814, July 2000.

[16] J. N. Kozhaya and F. N. Najm, "Power estimation for large sequential circuits," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, no. 2, pp. 400–407, April 2001.

[17] S. Bodapati and F. N. Najm, "Pre-layout estimation of individual wire lengths," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, no. 6, pp. 943–958, December 2001.

[18] V. Saxena, F. N. Najm, and I. N. Hajj, "Estimation of state line statistics in sequential circuits," *ACM Transactions on Design Automation of Electronic Systems*, vol. 7, no. 3, pp. 455–473, July 2002.

[19] S. Ramprasad, I. N. Hajj, and F. N. Najm, "A technique for improving dual-output domino logic," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 10, no. 4, pp. 508–511, August 2002.

[20] J. N. Kozhaya, S. R. Nassif, and F. N. Najm, "A multigrid-like technique for power grid analysis," *IEEE Transactions on Computer-Aided Design*, vol. 21, no. 10, pp. 1148–1160, October 2002.

[21] S. Gupta and F. N. Najm, "Energy and peak-current per-cycle estimation at RTL," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 4, pp. 525–537, August 2003.

[22] N. Azizi, F. N. Najm, and A. Moshovos, "Low-leakage asymmetric-cell SRAM," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 4, pp. 701–715, August 2003.

[23] J. H. Anderson and F. N. Najm, "Power estimation techniques for FPGAs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, no. 10, pp. 1015–1027, October 2004.

[24] A. Moshovos, B. Falsafi, F. N. Najm, and N. Azizi, "A case for asymmetric-cell cache memories," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 13, no. 7, pp. 877–881, July 2005.

[25] K. M. Buyuksahin and F. N. Najm, "Early power estimation for VLSI circuits," *IEEE Transactions on Computer-Aided Design*, vol. 24, no. 7, pp. 1076–1088, July 2005.

[26] I. A. Ferzli and F. N. Najm, "Analysis and verification of power grids considering process-induced leakage current variations," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 1, pp. 126–143, January 2006.

[27] J. H. Anderson and F. N. Najm, "Active leakage power optimization for FPGAs," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 3, pp. 423–437, March 2006.

[28] S. Bodapati and F. N. Najm, "High-level current macro-model for logic blocks," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 5, pp. 837–855, May 2006.

[29] B. Wu, J. Zhu, and F. N. Najm, "Dynamic range estimation," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 9, pp. 1618–1636, September 2006.

[30] D. Kouroussis, R. Ahmadi, and F. N. Najm, "Voltage-aware static timing analysis," *IEEE Transactions on Computer-Aided Design*, vol. 25, no. 10, pp. 2156–2169, October 2006.

[31] F. N. Najm, N. Menezes, and I. A. Ferzli, "A yield model for integrated circuits and its application to statistical timing Analysis," *IEEE Transactions on Computer-Aided Design*, vol. 26, no. 3, pp. 574–591, March 2007.

[32] N. Azizi, M. M. Khellah, V. De, and F. N. Najm, "Variations-aware low-power design and block clustering with voltage scaling," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 15, no. 7, pp. 746–757, July 2007.

[33] S. Onaissi and F. N. Najm, "A linear-time approach for static timing analysis covering all process corners," *IEEE Transactions on Computer-Aided Design*, vol. 27, no. 7, pp. 1291–1304, July 2008.

[34] K. R. Heloue and F. N. Najm, "Early analysis and budgeting of margins and corners using two-sided analytical yield models," *IEEE Transactions on Computer-Aided Design*, vol. 27, no. 10, pp. 1826–1839, October 2008.

[35] K. R. Heloue, N. Azizi, and F. N. Najm, "Full-chip model for leakage current estimation considering within-die correlation," *IEEE Transactions on Computer-Aided Design*, vol. 28, no. 6, pp. 847–887, June 2009.

[36] J. H. Anderson and F. N. Najm, "Low-power programmable FPGA routing circuitry," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 17, no. 8, pp. 1048–1060, August 2009.

[37] I. A. Ferzli, E. Chiprout, and F. N. Najm, "Verification and co-design of the package and die power delivery system using wavelets," *IEEE Transactions on Computer-Aided Design*, vol. 29, no. 1, pp. 92–102, January 2010.

[38] N. H. Abdul Ghani and F. N. Najm, "Fast vectorless power grid verification under an RLC model," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 30, no. 5, pp. 691–703, May 2011.

[39] H. Mangassarian, A. Veneris, and F. N. Najm, "Maximum circuit activity estimation using Boolean satisfiability," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 2, pp. 271–284, February 2012.

[40] K. R. Heloue, S. Onaissi, and F. N. Najm, "Efficient block-based parameterized timing analysis covering all potentially critical paths," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 31, no. 4, pp. 472–484, April 2012.

[41] S. Chatterjee, M. Fawaz, and F. N. Najm, "Redundancy-aware power grid electromigration checking under workload uncertainties," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 9, pp. 1509–1522, September 2015.

[42] M. Avci and F. N. Najm, "Verification of the power and ground grids under general and hierarchical constraints," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, No. 2, pp. 729–742, February 2016.

[43] Z. Moudallal and F. N. Najm, "Generating current budgets to guarantee power grid safety," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 35, no. 11, pp. 1914–1927, November 2016.

[44] M. Fawaz and F. N. Najm, "Fast vectorless RLC grid verification," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 3, pp. 489–502, March 2017.

[45] S. Chatterjee, V. Sukharev and F. N. Najm, "Power grid electromigration checking using physics-based models," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 7, pp. 1317–1330, July 2018. DOI: 10.1109/TCAD.2017.2666723 (Feb. 9, 2017)

[46] Z. Moudallal and F. N. Najm, "Generating current constraints to guarantee RLC power grid safety," *ACM Transactions on Design Automation of Electronic Systems (TODAES)*, Vol. 22, No. 4, pp. 66:1-66:39, June 2017.

[47] V. Sukharev and F. N. Najm, "Electromigration check: where the design and reliability methodologies meet," *IEEE Transactions on Device and Materials Reliability (TDMR)*, Vol. 18, No. 4, pp. 498–507, December 2018. DOI: 10.1109/TDMR.2018.2874244 (Oct. 5, 2018)

[48] Z. Moudallal and F. N. Najm, "Power scheduling with active RC power grids," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 27, No. 2, pp. 444–457, February 2019. DOI: 10.1109/TVLSI.2018.2877107 (Nov. 15, 2018)

[49] F. N. Najm and V. Sukharev, "Electromigration simulation and design considerations for integrated circuit power grids," *Journal of Vacuum Science & Technology B*, Vol. 38, No. 6, pp. 063204, October 2020. DOI: 10.1116/6.0000476 (Oct. 20, 2020).

[50] S. Torosyan, A. Kteyan, V. Sukharev, J.-H. Choy and F. N. Najm, "Novel physics-based tool-prototype for electromigration assessment in commercial- grade power delivery networks," *Journal of Vacuum Science & Technology B*, Vol. 39, No. 1, pp. 013203, January 2021. DOI: 10.1116/6.0000617 (Dec. 21, 2020).

Preprints and Magazine Articles

[1] F. Najm, "Estimating power dissipation in VLSI circuits," *IEEE Circuits and Devices Magazine*, vol. 10, no. 4, pp. 11–19, July 1994.

[2] F. Najm and J. Abraham, "Accounting for very deep sub-micron effects in silicon models," *EEDesign Magazine*, `http://www.eedesign.com/story/OEG20010109S1228`, Jan 09, 2001.

[3] A. Goyal and F. N. Najm, "Efficient RC power grid verification using node elimination," *Tech Design Forum*, `http://www.techdesignforums.com/eda/eda-topics/verified-rtl-to-gates/efficient-rc-power-grid-verification-using-node-elimination`, pp. 32–38, June 2011.

[4] F. N. Najm, "Model order reduction for lumped RC transmission lines," *TechRxiv*, October 17, 2020. DOI: 10.36227/techrxiv.13103294.v1 (preprint).

Conference Proceedings

[1] I. Hajj and F. Najm, "Test generation for physical faults in MOS VLSI circuits," *IEEE 1987 CompEuro Conference : VLSI & Computers*, Hamburg, West Germany, pp. 386–389, May 11–15, 1987.

[2] R. Burch, F. Najm, P. Yang, and D. Hocevar, "Pattern-independent current estimation for reliability analysis of CMOS circuits," *25th ACM/IEEE Design Automation Conference*, Anaheim, CA, pp. 294–299, June 12–15, 1988.

[3] F. Najm, R. Burch, P. Yang, and I. Hajj, "CREST - a current estimator for CMOS circuits," *IEEE International Conference on Computer-Aided Design*, Santa Clara, CA, pp. 204–207, November 7–10, 1988.

[4] F. Najm, I. Hajj, and P. Yang, "Electromigration median time-to-failure based on a stochastic current waveform," *IEEE International Conference on Computer-Design*, Cambridge, MA, pp. 447–450, October 2–4, 1989.

[5] F. Najm, I. Hajj, and P. Yang, "Computation of bus current variance for reliability estimation of VLSI circuits," *IEEE International Conference on Computer-Aided Design*, Santa Clara, CA, pp. 202–205, November 6–9, 1989.

[6] F. Najm and I. Hajj, "Probabilistic simulation of very large scale integrated circuits and systems," *1990 Bilkent International Conference on New Trends in Communications, Control, and Signal Processing*, Bilkent University, Ankara, Turkey, July 2–5, 1990.

[7] F. Najm, "Transition density, a stochastic measure of activity in digital circuits," *28th ACM/IEEE Design Automation Conference*, San Francisco, CA, pp. 644–649, June 17–21, 1991.

[8] H. Kriplani, F. N. Najm, and I. Hajj, "Maximum current estimation in CMOS circuits," *29th ACM/IEEE Design Automation Conference*, Anaheim, CA, pp. 2-7, June 8–12, 1992.

[9] R. Burch, F. Najm, P. Yang, and T. Trick, "McPOWER: A Monte Carlo approach to power estimation," *IEEE/ACM International Conference on Computer-Aided Design*, Santa Clara, CA, pp. 90-97, November 8–12, 1992.

[10] H. Kriplani, F. Najm, and I. Hajj, "Resolving signal correlations for estimating maximum currents in CMOS combinational circuits," *30th ACM/IEEE Design Automation Conference*, Dallas, TX, pp. 384–388, June 14–18, 1993.

[11] H. Kriplani, F. Najm, and I. Hajj, "Worst case voltage drops in power and ground buses of CMOS VLSI circuits," *SRC TECHON'93 Conference*, Atlanta, GA, pp. 402–404, September 28–30, 1993.

[12] F. Najm, "Improved Estimation of the Switching Activity for Reliability Prediction in VLSI Circuits," *IEEE Custom Integrated Circuits Conference*, San Diego, CA, pp. 429–432, May 1–4, 1994.

[13] M. Xakellis and F. Najm, "Statistical Estimation of the Switching Activity in Digital Circuits," *31st ACM/IEEE Design Automation Conference*, San Diego, CA, pp. 728–733, 1994.

[14] H. Kriplani, F. Najm, and I. Hajj, "Improved Delay and Current Models for Estimating Maximum Currents in CMOS VLSI Circuits," *IEEE International Symposium on Circuits and Systems*, vol. 1, pp. 435–438, 1994.

[15] F. N. Najm, "Towards a high-level power estimation capability," *IEEE International Symposium on Low Power Design*, Dana Point, CA, pp. 87–92, April 23–26, 1995.

[16] V. P. Dabholkar, S. Chakravarty, F. Najm, and J. Patel, "Cyclic stress tests for full scan circuits," *IEEE VLSI Test Symposium*, Princeton, NJ, pp. 89–94, April 30–May 3, 1995.

[17] R. Panda and F. N. Najm, "Technology decomposition for low-power synthesis," *IEEE Custom Integrated Circuits Conference*, Santa Clara, CA, pp. 627–630, May 1–4, 1995.

[18] F. N. Najm and M. Y. Zhang, "Extreme delay sensitivity and the worst-case switching activity in VLSI circuits," *ACM/IEEE Design Automation Conference*, San Francisco, CA, pp. 623–627, June 12–16, 1995.

[19] F. N. Najm, S. Goel, and I. N. Hajj, "Power estimation in sequential circuits," *ACM/IEEE Design Automation Conference*, San Francisco, CA, pp. 635–640, June 12–16, 1995.

[20] F. N. Najm, "Feedback, correlation, and delay concerns in the power estimation of VLSI circuits," *ACM/IEEE Design Automation Conference* **(Invited paper)**, San Francisco, CA, pp. 612–617, June 12–16, 1995.

[21] F. N. Najm, "Power Estimation Techniques for Integrated Circuits," *IEEE/ACM International Conference on Computer-Aided Design*, **(Invited tutorial paper)**, San Jose, CA, pp. 492–499, Nov. 5–9, 1995.

[22] M. Nemani and F. N. Najm, "High-Level Power Estimation and the Area Complexity of Boolean Functions," *IEEE International Symposium on Low Power Electronics and Design*, Monterey, CA, pp. 329-334, August 12–14, 1996.

[23] Luis E. Amaya, Philip T. Krein, and Farid N. Najm, "A Synthesis Environment for Power Electronics," *5th IEEE Workshop on Computers in Power Electronics*, Portland, OR, August 11–14, 1996

[24] V. Saxena, F. N. Najm, and I. N. Hajj, "Monte-Carlo approach for power estimation in sequential circuits," *European Design & Test Conference*, Paris, France, March 17–20, 1997.

[25] J. P. Halter and F. N. Najm, "A gate-level leakage power reduction method for ultra-low-power CMOS circuits," *IEEE Custom Integrated Circuits Conference*, Santa Clara, CA, pp. 475–478, May 5–8, 1997.

[26] M. Nemani and F. N. Najm, "High-level area prediction for power estimation," *IEEE Custom Integrated Circuits Conference*, Santa Clara, CA, pp. 483–486, May 5–8, 1997.

[27] S. Gupta and F. N. Najm, "Power macromodeling for high level power estimation," *34th Design Automation Conference*, pp. 365–370, Anaheim, CA, June 9–13, 1997.

[28] R. Panda and F. N. Najm, "Technology-dependent transformations for low-power synthesis," *34th Design Automation Conference*, pp. 650–655, Anaheim, CA, June 9–13, 1997.

[29] M. Nemani and F. N. Najm, "High-level area and power estimation for VLSI circuits," *IEEE/ACM International Conference on Computer-Aided Design*, pp. 114–119, Nov. 1997.

[30] J. Kozhaya and F. N. Najm, "Accurate power estimation for large sequential circuits," *IEEE/ACM International Conference on Computer-Aided Design*, pp. 488–493, Nov. 1997.

[31] M. Nemani and F. N. Najm, "Delay estimation for VLSI circuits from a high-level view," *35th Design Automation Conference*, pp. 591–594, San Francisco, CA, June 15–19, 1998.

[32] S. Gupta and F. N. Najm, "Analytical model for high level power modeling of combinational and sequential circuits," *IEEE Alessandro Volta Memorial Workshop on Low Power Design*, Como, Italy, pp. 164–172, March 4–5, 1999.

[33] S. Gupta and F. N. Najm, "Energy-per-cycle estimation at RTL," *IEEE International Symposium on Low Power Electronics and Design*, San Diego, CA, pp. 121–126, Aug. 16–17, 1999.

[34] S. Gupta and F. N. Najm, "Power macro-models for DSP blocks with application to high-level synthesis," *IEEE International Symposium on Low Power Electronics and Design*, San Diego, CA, pp. 103–105, Aug. 16–17, 1999.

[35] S. Ramprasad, I. N. Hajj, and F. N. Najm, "An optimization technique for dual-output domino logic," *IEEE International Symposium on Low Power Electronics and Design*, San Diego, CA, pp. 258–260, Aug. 16–17, 1999.

[36] G. Yoh and F. N. Najm, "A statistical model for electromigration failures," *IEEE 2000 1st International Symposium on Quality Electronic Design*, San Jose, CA, pp. 45–50, March 20–22, 2000.

[37] S. Bodapati and F. N. Najm, "Pre-layout estimation of individual wire lengths," *ACM International Workshop on System-Level Interconnect Prediction*, San Diego, CA, pp. 93-98, April 8–9, 2000.

[38] K. M. Buyuksahin and F. N. Najm, "High-level power estimation with interconnect effects," *IEEE International Symposium on Low Power Electronics and Design*, Italy, pp. 197–202, July 26–27, 2000.

[39] S. Bodapati and F. N. Najm, "Frequency-domain supply current macro-model," *IEEE International Symposium on Low Power Electronics and Design*, Huntington Beach, CA, pp. 295–298, Aug. 2001.

[40] J. N. Kozhaya, S. R. Nassif, and F. N. Najm, "I/O buffer placement methodology for ASICs," *8th IEEE International Conference on Electronics, Circuits and Systems*, Malta, pp. 245–248, Sept. 2001.

[41] M. Shahriari and F. N. Najm, "A gate-level timing model for SOI circuits," *8th IEEE International Conference on Electronics, Circuits and Systems*, Malta, pp. 795–798, Sept. 2001.

[42] J. N. Kozhaya, S. R. Nassif, and F. N. Najm, "Multigrid-like technique for power grid analysis," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, pp. 480–487, Nov. 2001.

[43] N. Azizi, A. Moshovos, and F. N. Najm, "Low-leakage asymmetric-cell SRAM," *ACM/IEEE International Symposium on Low Power Electronics and Design*, Monterey, CA, pp. 48–51, August 12–14, 2002.

[44] K. Buyuksahin and F. N. Najm, "High-level area estimation," *ACM/IEEE International Symposium on Low Power Electronics and Design*, Monterey, CA, pp. 271–274, August 12–14, 2002.

[45] J. H. Anderson and F. N. Najm, "Power-aware technology mapping for LUT-based FPGAs," *IEEE International Conference on Field-Programmable Technology*, Hong Kong, pp. 211–218, December 16–18, 2002.

[46] J. H. Anderson and F. N. Najm, "Switching activity analysis and pre-layout activity prediction for FPGAs," *ACM/IEEE International Workshop on System-Level Interconnect Prediction*, Monterey, CA, pp. 15–21, April 5–6, 2003.

[47] R. S. Guindi and F. N. Najm, "Design techniques for gate-leakage reduction in CMOS circuits," *IEEE International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, pp. 61–65, March 24–26, 2003.

[48] I. A. Ferzli and F. N. Najm, "Statistical estimation of leakage-induced power grid voltage drop considering within-die process variations," *ACM/IEEE 40th Design Automation Conference (DAC-03)*, Anaheim, CA, pp. 856–859, June 2-6, 2003.

[49] D. Kouroussis and F. N. Najm, "A static pattern-independent technique for power grid voltage integrity verification," *ACM/IEEE 40th Design Automation Conference (DAC-03)*, Anaheim, CA, pp. 99–104, June 2-6, 2003.

[50] R. S. Guindi, R. C. Kordasiewicz, and F. N. Najm, "Optimization technique for FB/TB assignment in PD-SOI digital CMOS circuits," *The First Annual Northeast Workshop on Circuits and Systems (NEWCAS)*, Montreal, Quebec, Canada, pp. 157–160, June 17–20, 2003.

[51] R. Ahmadi and F. N. Najm, "Timing analysis in presence of power supply and ground voltage variations," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, pp. 176–183, November 9-13, 2003.

[52] I. A. Ferzli and F. N. Najm, "Statistical verification of power grids considering process-induced leakage current variations," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, pp. 770–777, November 9–13, 2003.

[53] J. H. Anderson and F. N. Najm, "Interconnect capacitance estimation for FPGAs," *IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC)*, Yokohama, Japan, pp. 713–718, January 27–30, 2004.

[54] J. H. Anderson, F. N. Najm, and T. Tuan, "Active leakage power optimization for FPGAs," *ACM/SIGDA International Symposium on Field Programmable Gate Arrays (FPGA)*, Monterey, CA, pp. 33–41, February 22–24, 2004.

[55] N. Azizi and F. N. Najm, "An asymmetric SRAM cell to lower gate leakage," *IEEE International Symposium on Quality Electronic Design (ISQED)*, San Jose, CA, pp. 534–539, March 22–24, 2004.

[56] I. A. Ferzli and F. N. Najm, "Statistical estimation of circuit timing vulnerability due to leakage-induced power grid voltage drop," *IEEE International Conference on Integrated Circuit Design and Technology (ICICDT)*, Austin, TX, pp. 17–24, May 17–20, 2004 **(Invited Paper)**.

[57] F. N. Najm and N. Menezes, "Statistical timing analysis based on a timing yield model," *ACM/IEEE 41st Design Automation Conference (DAC)*, San Diego, CA, pp. 460–465, June 7–11, 2004.

[58] B. Wu, J. Zhu, and F. N. Najm, "An analytical approach for dynamic range estimation," *ACM/IEEE 41st Design Automation Conference (DAC)*, San Diego, CA, pp. 472–477, June 7–11, 2004.

[59] D. Kouroussis, R. Ahmadi, and F. N. Najm, "Worst-case circuit delay taking into account power supply variations," *ACM/IEEE 41st Design Automation Conference (DAC)*, San Diego, CA, pp. 652–657, June 7–11, 2004.

[60] D. Kouroussis, R. Ahmadi, and F. N. Najm, "A worst-case circuit delay verification technique considering power grid voltage variations," *The 2nd Annual Northeast Workshop on Circuits and Systems (NEWCAS-04)*, Montreal, Quebec, pp. 157–160, June 20–23, 2004.

[61] J. H. Anderson and F. N. Najm, "A Novel Low-Power FPGA Routing Switch," *IEEE Custom Integrated Circuits Conference (CICC)*, Orlando, FL, pp. 719–722, October 3–6, 2004.

[62] J. H. Anderson and F. N. Najm, "Low-power programmable routing circuitry for FPGAs," *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, pp. 602–609, November 7–11, 2004.

[63] B. Wu, J. Zhu, and F. N. Najm, "Dynamic range estimation for nonlinear systems," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, San Jose, CA, pp. 660-667, November 7–11, 2004.

[64] N. Azizi, M. M. Khellah, V. De, and F. N. Najm, "Variations-aware low-power design with voltage scaling," *ACM/IEEE 42nd Design Automation Conference (DAC-05)*, Anaheim, CA, pp. 529–534, June 13–17, 2005.

[65] F. N. Najm, "On the need for statistical timing analysis," *ACM/IEEE 42nd Design Automation Conference (DAC-05)*, Anaheim, CA, pp. 764–765, June 13–17, 2005.

[66] B. Wu, J. Zhu, and F. N. Najm, "A non-parametric approach for dynamic range estimation of nonlinear systems," *ACM/IEEE 42nd Design Automation Conference (DAC-05)*, Anaheim, CA, pp. 841–844, June 13–17, 2005.

[67] N. Azizi and F. N. Najm, "Compensation for within-die variations in dynamic logic by using body-bias," *Northeast Workshop on Circuits and Systems (NEWCAS-05)*, Quebec City, QC, Canada, pp. 167–170, June 19–22, 2005.

[68] G. Nabaa and F. N. Najm, "Minimization of delay sensitivity to process induced voltage threshold variations," *Northeast Workshop on Circuits and Systems (NEWCAS-05)*, Quebec City, QC, Canada, pp. 171–174, June 19–22, 2005.

[69] K. R. Heloue and F. N. Najm, "Effect of statistical clock skew variations on chip timing yield," *Northeast Workshop on Circuits and Systems (NEWCAS-05)*, Quebec City, QC, Canada, pp. 211–214, June 19–22, 2005.

[70] M. Nizam, F. N. Najm, and A. Devgan, "Power grid voltage integrity verification," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED-05)*, San Diego, CA, pp. 239–244, August 8–10, 2005.

[71] N. Azizi and F. N. Najm, "Look-up table leakage reductions for FPGAs," *IEEE Custom Integrated Circuits Conference (CICC-05)*, San Jose, CA, pp. 187–190, September 18–21, 2005.

[72] D. Kouroussis, I. A. Ferzli, and F. N. Najm, "Incremental partitioning-based vectorless power grid verification," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-05)*, San Jose, CA, pp. 358–364, November 6–10, 2005.

[73] K. R. Heloue and F. N. Najm, "Statistical timing analysis with two-sided constraints," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-05)*, San Jose, CA, pp. 829–836, November 6–10, 2005.

[74] G. Nabaa, N. Azizi, and F. N. Najm, "An adaptive FPGA architecture with process variation compensation and reduced leakage," *ACM/IEEE 43rd Design Automation Conference (DAC-06)*, San Francisco, CA, pp. 624–629, July 24–28, 2006.

[75] N. Azizi, and F. N. Najm, "A family of cells to reduce the soft-error-rate in ternary-CAM," *ACM/IEEE 43rd Design Automation Conference (DAC-06)*, San Francisco, CA, pp. 779–784, July 24–28, 2006.

[76] K. Pagiamtzis, N. Azizi, and F. N. Najm, "A soft-error tolerant content-addressable memory (CAM) using an error-correcting-match scheme," *IEEE Custom Integrated Circuits Conference (CICC-06)*, San Jose, CA, pp. 301–304, September 10–13, 2006.

[77] N. H. Abdul Ghani and F. N. Najm, "Handling inductance in early power grid verification," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-06)*, San Jose, CA, pp. 127–134, November 5–9, 2006.

[78] S. Onaissi and F. N. Najm, "A Linear-Time Approach for Static Timing Analysis Covering All Process Corners," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-06)*, San Jose, CA, pp. 217–224, November 5–9, 2006.

[79] H. Mangassarian, A. Veneris, S. Safarpour, F. N. Najm, and M. S. Abadir, "Maximum circuit activity estimation using pseudo-Boolean satisfiability," *Design, Automation and Test in Europe (DATE-07)*, Nice, France, pp. 1538–1543, April 16–20, 2007.

[80] N. Azizi and F. N. Najm, "Using keeper control and body bias for fine grained threshold voltage compensation in dynamic logic," *20th Canadian Conference on Electrical and Computer Engineering*, Vancouver, BC, pp. 1639–1644, April 22–26, 2007.

[81] K. R. Heloue and F. N. Najm, "Early statistical timing analysis with unknown within-die correlations," *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU-07)*, Austin, TX, pp. 13–18, February 26–27, 2007.

[82] K. R. Heloue and F. N. Najm, "Early analysis of timing margins and yield," *20th Canadian Conference on Electrical and Computer Engineering*, Vancouver, BC, pp. 1114–1120, April 22–26, 2007.

[83] K. R. Heloue, N. Azizi, and F. N. Najm, "Modeling and Estimation of Full-Chip Leakage Current Considering Within-Die Correlation," *ACM/IEEE 44th Design Automation Conference (DAC-07)*, San Diego, CA, pp. 93–98, June 4–8, 2007.

[84] I. A. Ferzli, F. N. Najm, and L. Kruse, "Early power grid verification under circuit current uncertainties," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED-07)*, Portland, OR, pp. 116–121, August 27–29, 2007.

[85] I. A. Ferzli, F. N. Najm, and L. Kruse, "A geometric approach for early power grid verification using current constraints," *ACM/IEEE International Conference on Computer-Aided Design (ICCAD-07)*, San Jose, CA, pp. 40–47, November 5–8, 2007.

[86] K. R. Heloue and F. N. Najm, "Parameterized timing analysis with general delay models and arbitrary variation sources," *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU-08)*, Monterey, CA, pp. 14–19, February 25–26, 2008.

[87] K. R. Heloue and F. N. Najm, "Parameterized timing analysis with general delay models and arbitrary variation sources," *ACM/IEEE 45th Design Automation Conference (DAC-08)*, Anaheim, CA, pp. 403–408, June 8–13, 2008.

[88] I. A. Ferzli, E. Chiprout, and F. N. Najm, "Verification and co-design of the package and die power delivery system using wavelets," *IEEE Conference on Electrical Performance of Electronic Packaging (EPEP)*, San Jose, CA, pp. 7–10, October 27–29, 2008.

[89] K. R. Heloue, S. Onaissi, and F. N. Najm, "Efficient block-based parameterized timing analysis covering all potentially critical paths," *ACM/IEEE International Conference on Computer-Aided Design (ICCAD-08)*, San Jose, CA, pp. 173–180, November 10–13, 2008.

[90] K. R. Heloue, C. V. Kashyap, and F. N. Najm, "Quantifying robustness metrics in parameterized static timing analysis," *ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU-09)*, Austin, TX, pp. 49–54, February 23–24, 2009.

[91] N. H. Abdul Ghani and F. N. Najm, "Fast vectorless power grid verification using an approximate inverse technique," *ACM/IEEE 46th Design Automation Conference (DAC-09)*, San Francisco, CA, pp. 184–189, July 26–31, 2009.

[92] S. Onaissi, K. R. Heloue, and F. N. Najm, "Clock skew optimization via wiresizing for timing sign-off covering all process corners," *ACM/IEEE 46th Design Automation Conference (DAC-09)*, San Francisco, CA, pp. 196–201, July 26–31, 2009.

[93] K. R. Heloue, C. V. Kashyap, and F. N. Najm, "Quantifying robustness metrics in parameterized static timing analysis," *ACM/IEEE International Conference on Computer-Aided Design (ICCAD-09)*, San Jose, CA, pp. 209–216, November 2–5, 2009.

[94] S. Onaissi, K. R. Heloue, and F. N. Najm, "PSTA-based branch and bound approach to the Silicon speedpath isolation problem," *ACM/IEEE International Conference on Computer-Aided Design (ICCAD-09)*, San Jose, CA, pp. 217–224, November 2–5, 2009.

[95] S. Safarpour, A. Veneris, and F. N. Najm, "Managing verification error traces with bounded model debugging," *The 15th Asia and South Pacific Design Automation Conference (ASP-DAC)*, Taipei, Taiwan, pp. 601–606, Jan. 18–21, 2010.

[96] M. Aydonat and F. N. Najm, "Power grid correction using sensitivity analysis," *ACM/IEEE International Conference on Computer-Aided Design (ICCAD-10)*, San Jose, CA, pp. 808-815, November 7–11, 2010.

[97] M. Avci and F. N. Najm, "Early P/G grid voltage integrity verification," *ACM/IEEE International Conference on Computer-Aided Design (ICCAD-10)*, San Jose, CA, pp. 816-823, November 7–11, 2010.

[98] A. Goyal and F. N. Najm, "Efficient RC power grid verification using node elimination," *Design, Automation and Test in Europe (DATE-11)*, Grenoble, France, pp. 257–260, March 14–18, 2011.

[99] N. H. Abdul Ghani and F. N. Najm, "Power grid verification using node and branch dominance," *ACM/IEEE 47th Design Automation Conference (DAC-2011)*, San Diego, CA, pp. 682–687, June 5–9, 2011.

[100] P. Al Haddad and F. N. Najm, "Power grid correction using sensitivity analysis under an RC model," *ACM/IEEE 47th Design Automation Conference (DAC-2011)*, San Diego, CA, pp. 688–693, June 5–9, 2011.

[101] S. Onaissi, F. Taraporevala, J. Liu, and F. N. Najm, "A fast approach for static timing analysis covering all PVT corners," *ACM/IEEE 47th Design Automation Conference (DAC-2011)*, San Diego, CA, pp. 777–782, June 5–9, 2011.

[102] Abhishek and F. N. Najm, "Incremental power grid verification," *ACM/IEEE 48th Design Automation Conference (DAC-2012)*, San Francisco, CA, pp. 151–156, June 3–7, 2012.

[103] F. N. Najm, "Overview of vectorless/early power grid verification," *ACM/IEEE International Conference on Computer-Aided Design* **(Invited paper)**, San Jose, CA, pp. 670–677, November 5–8, 2012.

[104] S. Chatterjee, M. Fawaz, and F. N. Najm, "Redundancy-aware electromigration checking for mesh power grids," *ACM/IEEE International Conference on Computer-Aided Design (ICCAD-13)*, San Jose, CA, pp. 540–547, November 18–21, 2013.

[105] M. Fawaz, S. Chatterjee, and F. N. Najm, "A vectorless framework for power Grid electromigration checking," *ACM/IEEE International Conference on Computer-Aided Design (ICCAD-13)*, San Jose, CA, pp. 553–560, November 18–21, 2013.

[106] Z. Moudallal and F. N. Najm, "Generating circuit current constraints to guarantee power grid Safety," *20th Asia and South Pacific Design Automation Conference (ASP-DAC '15)*, Chiba/Tokyo, Japan, pp. 358–365, January 19–22, 2015.

[107] M. Fawaz and F. N. Najm, "Accurate verification of RC power grids," *Design, Automation and Test in Europe (DATE-16)*, Dresden, Germany, pp. 814–817, March 14–18, 2016.

[108] M. Fawaz and F. N. Najm, "Fast simulation-based verification of RC power grids, " *IEEE Canadian Conference on Electrical and Computer Engineering (CCECE-16)*, Vancouver, Canada, pp. 1182–1187, May 15–18, 2016.

[109] Z. Moudallal and F. N. Najm, "Generating voltage drop aware current budgets for RC power grids," *IEEE International Symposium on Circuits and Systems (ISCAS-16)*, Montreal, Canada, pp. 2583–2586, May 22–26, 2016.

[110] A.-A. Yassine and F. N. Najm, "A fast layer elimination approach for power grid reduction," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-16)*, Austin, TX, pp. 8B.4, November 7–10, 2016.

[111] S. Chatterjee, V. Sukharev and F. N. Najm, "Fast physics-based electromigration checking for on-die power grids," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-16)*, Austin, TX, pp. 9A.1, November 7–10, 2016. **(Best Paper Award)**

[112] V. Sukharev, A. Kteyan, J.-H. Choy, S. Chatterjee and F. N. Najm, "Theoretical predictions of EM-induced degradation in test-structures and on-chip power grids with analytical and numerical analysis," *IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, pp. 6B.5, April 2–6, 2017. **(Invited Paper)**

[113] M. Fawaz and F. N. Najm, "Parallel simulation-based verification of RC power grids," *IEEE Computer Society Annual Symposium on VLSI*, Bochum, Germany, pp. 445–452, July 3–5, 2017.

[114] J.-H. Choy, V. Sukharev, S. Chatterjee, F. N. Najm, A. Kteyan and S. Moreau, "Finite-difference methodology for full chip electromigration analysis applied to a 3D IC test structure: Simulation vs. experiment," *IEEE International Conference on Simulation of Semiconductor Processes and Devices (SISPAD-17)*, Kamakura, Japan, pp. 41–44, September 7–9, 2017.

[115] Z. Moudallal and F. N. Najm, "Power scheduling with active power grids," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-17)*, Irvine, CA, pp. 466–473, November 13–16, 2017.

[116] M. Fawaz and F. N. Najm, "Power grid verification under transient constraints," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-17)*, Irvine, CA, pp. 593–600, November 13–16, 2017.

[117] S. Chatterjee, V. Sukharev and F. N. Najm, "Fast physics-based electromigration assessment by efficient solution of linear time-invariant (LTI) systems," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-17)*, Irvine, CA, pp. 659–666, November 13–16, 2017.

[118] F. N. Najm and V. Sukharev, "Efficient simulation of electromigration damage in large chip power grids using accurate physical models," *IEEE International Reliability Physics Symposium (IRPS-19)*, Monterey, CA, pp. 2A.1-1 – 2A.1-10, March 31 - April 3, 2019. **(Invited Paper)**

[119] Z. Moudallal, V. Sukharev and F. N. Najm, "Power grid fixing for electromigration-induced voltage failures," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-19)*, Westminster, CO, November 4–7, 2019. **(Best Paper Award)**

[120] A. Issa, V. Sukharev and F. N. Najm, "Electromigration checking using a stochastic effective current model," *IEEE/ACM International Conference on Computer-Aided Design (ICCAD-20)*, November 2–5, 2020. **(Best Paper Award)**

Are you looking for Personal background images? Pikbest have found 3332 great Personal Background for website,desktop and advertisement design. More HD background could be used personal and commercial free Download,Please visit pikbest.com. A personal background check is a consumer-level background check that allows job seekers to view general information about themselves online. Although it is wise for job seekers to run personal background checks on themselves, they should be aware of the type of information it will show them. Personal background checks are often limited in the information they can reveal, unlike the extensive background screening that employers have access to. 1 right click, personalise. desktop background, browse for your images (which you saved as a 'Save for web' image in photoshop). click on it, select the lefternmost tick box at the bottom, then click ok. looks snazzy doesn't it Add Tip. Ask Question. Comment. Download.