# A CAD Tool for Automated Design of Low-noise Nullor Based Amplifiers

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***Abstract*— Low Noise Amplifiers (LNA's) have become important for wideband-ultrawideband radio, microwave and cell-phone designers. In the design methodology, the LNA is composed by a nullor which represents an ideal active gain, i.e. the plant to be controlled by the feedback network which is usually constituted by passive components.**
**The paper shows that the noise calculation for these passive components and the synthesis of the first stage of the nullor can be automatically done. The automation is verified by means of a program that designs the feedback network and selects the right device to accomplish the noise specs provided by the designer.**

## I. Introduction

The low noise amplifier is a system where the noise level is carefully handled; it is usually the first block in a radio receiver that amplifies the signal from the antenna with as little distortion and additional noise as possible to be suitable for being processed by the first mixer [1].

The design of analogue electronic circuits has often been classified as an art under the assumption that no systematic procedures or methodologies have been developed. Experience has been the major way to produce knowledge regarding analogue design. The traditional way to obtain a new design is by carrying out some modifications on an already existing circuit until it fulfils some specific features. Nevertheless this way of design results very cryptic and difficult to handle for students and young designers.

Structured design has raised as an alternative to accomplish the analogue design task. It is based on the concept that the design must start from an ideal solution — which obviously fulfils any set of specifications. The structured design is oriented to optimise aspects such as noise, distortion and bandwidth from a block point of view [2], [3]. This approach lets the designer to focus on only one design aspect at a time [4].

This work is focused on the first block to be designed which is the noise block. The noise stage is always the first to be designed because main noise contributions come from this block. If we consider the blocks of Figure 1; when a resistance is reflected from the output to the input of the first block, the resistance is diminished by a value equal to the square of the gain. Then if a resistance is reflected from the output circuit of the second block to the input of the first block, then the resistance is diminished by the product of the squares of the individual gains [5]. Therefore, the equivalent noise resistance

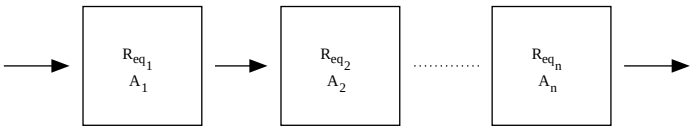


Fig. 1. Cascade of multiple stages.

of the block combination is be given by

$$R_{eq_T} = R_{eq_1} + \frac{R_{eq_2}}{{A_1}^2} + ... + \frac{R_{eq_n}}{({A_1}^2)...({A_n}^2)} \qquad (1)$$

In fact, this means that the main noise contribution belongs to the first block of the design.

## II. Nullor-based amplifiers

Within the structured design methodology, the nullor constitutes the active (ideal) block of the amplifier. The nullor is a two-port composed by two elements: **the nullator** connected at the input port and **the norator** connected at the output port. The transmission matrix of the nullor is given as [6], [7]:

$$K = \begin{bmatrix} \frac{1}{\mu} & \frac{1}{\gamma} \\ \\ \frac{1}{\zeta} & \frac{1}{\beta} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \qquad (2)$$

It clearly results that the nullor possesses infinite gains for all four transfer relationships, voltage ($\mu$), current ($\alpha$), trans-conductance ($\gamma$) and trans-impedance ($\zeta$).

The basic one-loop amplifiers can be obtained when a passive feedback network is connected with the nullor as shown in Figure 2. If the one-loop amplifiers are combined then two basic two-loop types of amplifiers are generated as shown in Figure 3. The combination of voltage amplifier and current amplifier are referred as the **two-loop topology (A)** and the combination of transconductance and transimpedance amplifiers are denoted as the **two-loop topology (B)** [3], [4].

Topology (B) can achieve all four kinds of transfers (voltage, current, transconductance and transimpedance), while Topology (A) can achieve all but the transconductance.

### *A. Noise in the Amplifier*

In order to evaluate the noise in active devices the concept of noise factor is still widely used. The noise factor (*F*) is a quantity that compares the noise performance of a device against an ideal (noiseless) device. The noise power output

of an ideal device is due to the thermal noise power of the source resistance [8]. Noise factor expressed in decibels is called noise figure (*NF*) and is expressed as:

$$NF = 10log_{10}F \tag{3}$$

Noise can be regarded in terms of power spectral densities originated from the passive network and the synthesised nullor. Because structured design uses power spectral densities for noise calculations then it is necessary to convert the noise figure term for the active devices into a noise voltage and current model, this method is explained in [8].

A high-performance feedback amplifier accomplishes a specified transfer of a signal obtained from a signal source with known impedance to the load, while preserving the quality of the signal as much as possible. The feedback network affects the noise contribution of the noise sources present in the active circuit, usually increasing their contribution. The noise introduced by the transistor stages can be represented by a current and a voltage source placed at the input of the active part.

The method to obtain the equivalent input noise sources for the single-loop topologies is detailed in [9], for the two-loop topologies a similar approach is used although it results rather cumbersome. The overall noise of the amplifier consists of two contributions. The first contribution comes from the feedback network, while the second contribution comes from the active devices.

Because the structured design constitutes in fact the systematic synthesis of the nullor with active devices (BJT or MOS transistors), noise design at the beginning of the process must perform a careful selection of the device which leads to an adequate calculation of bias value.

MOSFET's are considered less suitable due to their large excess-noise contribution. For each transistor the voltage and current noise contributions are determined by the parameters and the bias current of the transistor [4]. The optimal first stage of the active circuit can be found by determining the optimal bias current. This is done by performing calculations that

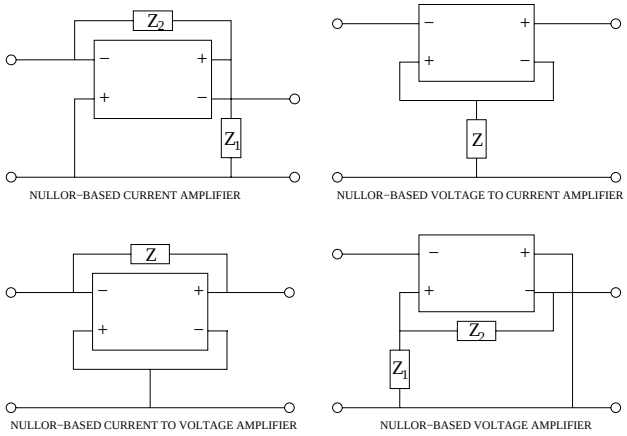


Fig. 2. Negative-feedback Amplifiers.

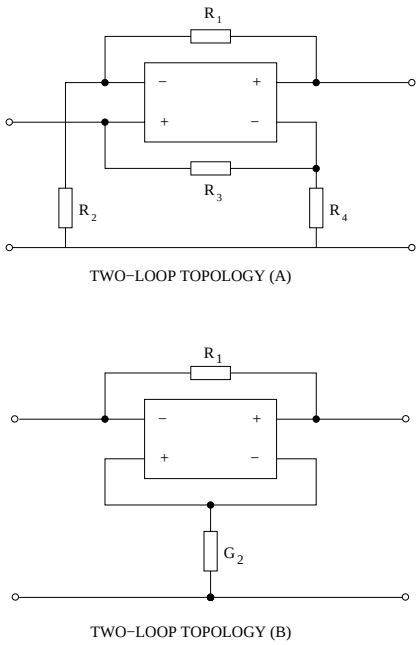


Fig. 3. Two-loop Amplifiers.

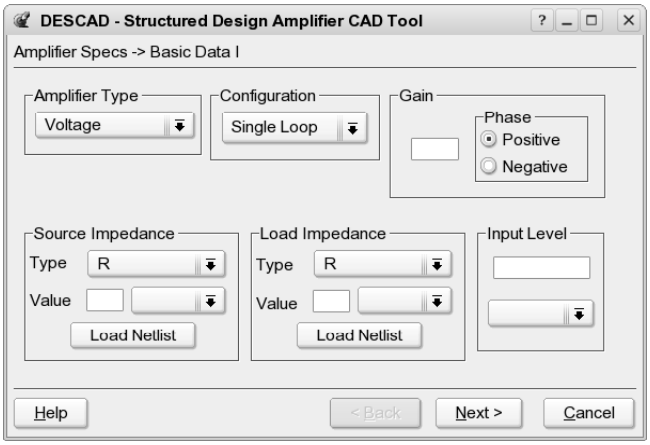


Fig. 4. Initial screen for NOMAD wizard.

involve the internal parameters of the device ($g_m$, internal base resistance, collector resistance), the source signal (internal resistance) and the supply source.

An adequate bias value means that the noise contributed by the active device, the feedback-network and source complies at least to the noise limit established by the designer.

## III. Program Structure

A CAD tool — **NOMAD (Noise Optimisation in Modern Amplifier Design)** — is aimed to simplify and automate the design process of negative-feedback amplifiers based on nullors. The designer provides a set of specifications such as amplifier transfer, configuration, gain, bandwidth and maximum allowed noise level among others.

The tool has been developed in C++ for the backend, while the graphical user interface is programmed in Qt. The tool is

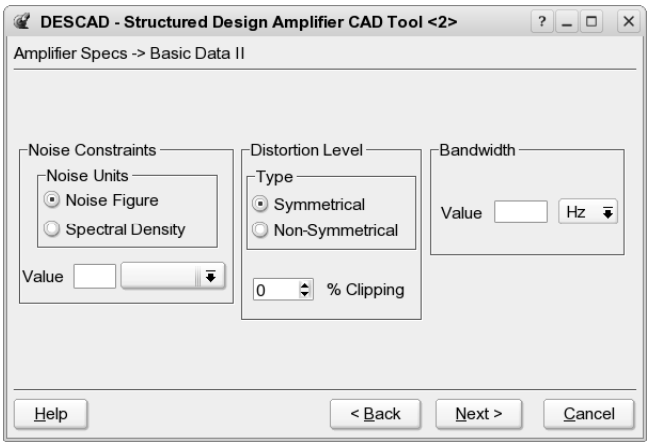


Fig. 5. Second window for NOMAD wizard.

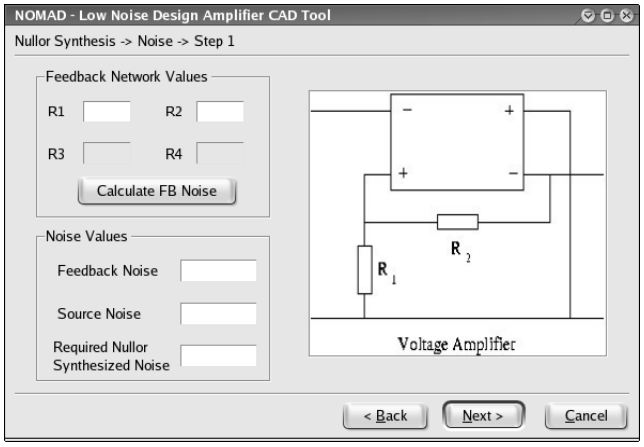


Fig. 6. Feedback noise calculation.

aimed to run under Linux/Solaris without any constraints for special libraries.

The main idea about the program is to guide the designer through the design process by means of a wizard approach. This wizard resorts to the use of windows as seen in Figure 4. The initial window is devoted to introduce the amplifier basic specs like the amplifier type, configuration, amplifier gain, source impedance, and load impedance.

The second window, Figure 5, expects three values to be specified: distortion, bandwidth, and noise constraints. Noise value can be given in two different units. Noise figure value is given in decibel units while spectral density is given by $\frac{V}{\sqrt{Hz}}$ or $\frac{A}{\sqrt{Hz}}$.

Once the basic specs have been provided, the program performs the required calculations for the feedback network. This is displayed on a third window, entitled **Noise, Step 1** (Figure 6). In order to accomplish the maximum allowed noise level it is necessary to have a trade-off between the noise contribution from the feedback network and the noise contribution from the active device that synthesizes the nullor.

Figure 7 shows the window entitled **Noise, Step 2**. Here the designer can select between some transistor configurations

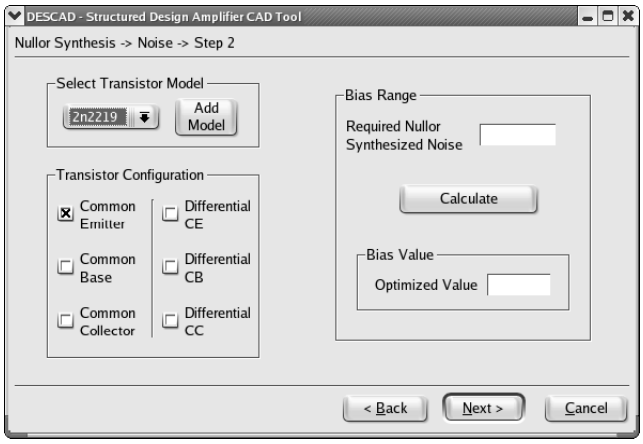


Fig. 7. Active device noise calculation.

(common emitter, common base, common collector, differential common emitter, differential common base, differential common collector). By clicking the **Calculate** button a bias optimisation process is activated, and the value for optimum Ic is displayed. In case this process fails, a warning message is issued and the design process restarted from the first screen.

For the noise calculations on resistors and active devices SPICE-like calculations are performed [10]. The equations and the values obtained using them were validated after performing simulations on APLAC [11] which includes a model that resembles the nullor behaviour. NOMAD finishes after delivering the final result for the amplifier, i.e. the value of the feedback resistors, the data regarding the active device parameters and the required bias current.

## IV. Example

A design example is provided in order to show the function of the tool. The amplifier to be designed must fulfil these specs:

- Type = Voltage Amplifier
- Configuration = Single Loop
- Gain = 17 dB
- Noise Figure = 2 dB
- BW = 441 – 451 MHz
- Source Impedance= 100 Ω

The calculated values for the feedback network are (Figure 6):

- R1 = 25 Ω
- R2 = 150 Ω

Noise figure for the feedback network and source is 0.84 dB. Next step is to select the active device, configuration and then calculate the appropriate bias current.

The selected device is a BJT BFR520 [12] in common emitter configuration. This device has an excellent low-noise figure performance and is adequate for RF wideband applications. The selected bias current value is 3.4 mA. The noise figure for this bias value is 1.03dB. The total noise figure for the amplifier is 1.7 dB, this means that the tool can compute

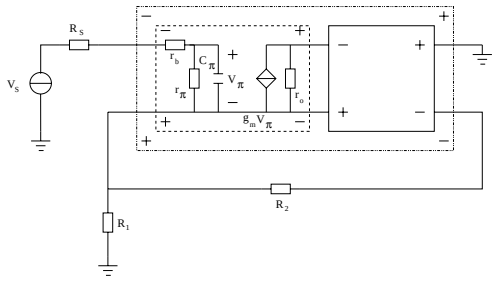


Fig. 8. Schema to simulate the nullor implementation.

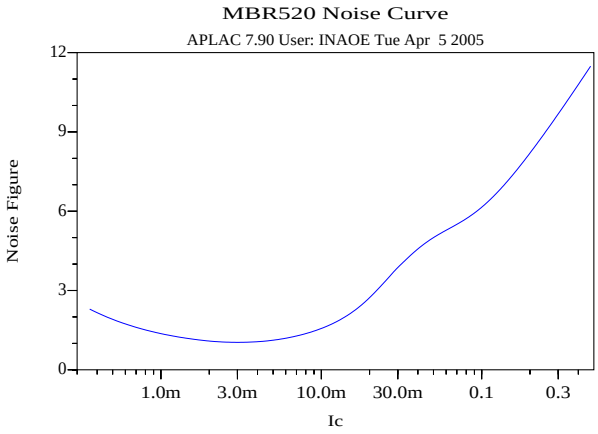


Fig. 9. Noise figure versus collector current.

the adequate values for the resistors and bias value for the active device.

In order to verify if the design has fulfilled the specs, the resulting amplifier is simulated in APLAC. The schema is shown in Figure 8. The nullor is replaced by an ideal op-amp, though this element is not a nullor, its behaviour is the closest to it. Figure 9 shows that the bias value for the BFR520 is the optimum to obtain the lowest noise figure. Figure 10 shows the noise behaviour against frequency. As we can see this amplifier is within limits for a low-noise amplifier and accomplish the given specs.

## V. Conclusion

It has been shown that it is possible to develop a CAD tool oriented to automate the design of low noise amplifiers based on a set of specifications provided by the designer. By means of a wizard approach the tool guides the designer in entering the amplifier specs in a step-by-step procedure. In case that the specs can not be fulfilled, the design process is stopped and taken to a previous step to modify one or more values. The development of the tool is based entirely on structured design, this shows that this design approach can speed up the design process obtaining accurate results.

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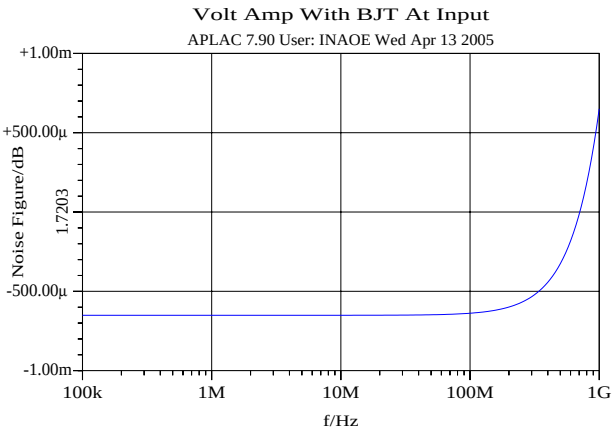


Fig. 10. Frequency behaviour for voltage amplifier.

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The method is applied to the design of inductive source degenerated common source amplifiers at the 90 nm and 180 nm technology nodes. The optimization results are validated through comparison with numerical simulations using Agilentâ€™s Advanced Design Systems (ADS) software.Â  Efficient and accurate optimization techniques for implementing analog integrated circuits are a critical facet of a CAD-based design flow. This is essential when the goal is to minimize the time-to-market for a product, and thus have working designs on first silicon [10]. While the noise analysis of a linear two-port network provides some insight into how to optimize the noise figure (NF) of an amplifier [11], this classical approach does not provide any guidance on the sizing of the devices. K-Band Low-Noise Amplifier Design in CMOS Technology. by. Dustin Dunwell.Â  More recently, advances in the CAD tools used to help model the properties of integrated circuit components, such as three-dimensional numerical simulators, have enabled the accurate prediction and Q factor optimization of spiral inductors for frequencies up to 5 GHz [5]. As CMOS operating frequencies continue to increase, however, spiral inductor modeling techniques have struggled to keep up due to the complexity.Â  Receiver Antenna. Lowâˆ’Noise Amplifier. Mixer. IF Amplifier. 8. DSP. 4. Practical recommendations for design of low noise amplifiers Every resistor is a noise source so it is necessary to keep all resistors in a signal path (and also signal source resistance) on very low level otherwise low noise performance of any amplifier will be wasted. Proper supply decoupling (omitted for clarity) is necessary. Parallel combination of large electrolytic cap 470uF with several 100nF-10uF ceramic in every supply with serial resistor 47-100 Ohm is recommended. If switching regulators are used, additional RC/LC filter is essential. A PCB with at least 2 layers and solid groun This paper presents a set of CAD tools for computer-aided design of CMOS switched-capacitor (SC) EA modulators. They cover optimization at the modulator and cell levels, advanced behavioral simulation at the modulator level, and the capability to explore design spaces for modulator architectures. These sets of tools are vertically integrated to support topdown design of SC CA modulators, from the high-level specifications to the sizes of the analog cells, which is demonstrated in the paper through two silicon prototypes in 1.2 pm CMOS technology.Â  The equivalent level of white noise is first calculated based on accurate analytical expressions for standard SC multibranch integrators and then added in time-domain to the integrator input using a random number generator.